AMENDMENTS TO THE CLAIMS

Claims 10, 12-15 and 26-27 are pending in the Application. Claim 10 is an independent claim and claim 12 depends therefrom. Claim 13 is an independent claim and claims 14-15 depend therefrom. Claims 26 is an independent claim and claim 27 depends therefrom. Claims 11, 16-23, 25 and 28-40 were previously canceled. Claims 1-9 and 25 are currently canceled. Claim 27 is currently amended.

Listing of Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

1-9. (Canceled)

10. (Previously Presented) A memory management circuit for managing a memory having a plurality of memory blocks, each memory block having a plurality of memory segments, the memory management circuit comprising:

a first logic circuit associated exclusively with a first memory block of the plurality of memory blocks, the first logic circuit having a first state when any of the memory segments of the first memory block are available for data storage and a second state when none of the memory segments of the first memory block are available for storage;

a second logic circuit having a first state when a first memory segment of the first memory block is available for data storage and a second state when the first memory segment of the first memory block is not available for data storage; and

a third logic circuit having a first state when a second memory segment of the first memory block is available for data storage and a second state when the second memory

segment of the first memory block is not available for data storage;

wherein the first state of the first logic circuit comprises a number of available memory segments in the first memory block, said number of available memory segments corresponding to at least the first state of the second logic circuit and the first state of the third logic circuit,

wherein the first state of the first logic circuit is separate from the first state of the second logic circuit and the first state of the third logic circuit.

11. (Canceled)

12. (Previously Presented) The memory management circuit of claim 10, wherein the first and second states of the second and third logic circuits are single-bit logic states.

13. (Previously Presented) A memory management circuit for managing a memory having a plurality of memory blocks, each memory block having a plurality of memory segments, the memory management system comprising:

a first logic circuit associated exclusively with a first memory block of the plurality of memory blocks, the first logic circuit having a first state when any of the memory segments of the first memory block are available for data storage and a second state when none of the memory segments of the first memory block are available for storage;

wherein the second state of the first logic circuit comprises an offset to available memory.

14. (Previously Presented) The memory management circuit of claim 13, further comprising a second logic circuit having a first state when a first memory segment of the first memory block is available for data storage and a second state when the first memory segment of the first memory

block is not available for storage.

15. (Previously Presented) The memory management system of claim 14, wherein the second state of the second logic circuit comprises an offset to an available memory segment.

16-25. (Canceled)

26. (Previously Presented) A method for managing memory, the method comprising:

analyzing a state of a first logic circuit to determine whether a block of memory segments includes a memory segment that is available for data storage, the first logic circuit having a first state when the block of memory segments has a memory segment that is available for data storage and a second state when the block of memory segments does not have a memory segment that is available for data storage; and

if the block of memory segments includes a memory segment that is available for data storage, identifying a memory segment in the block of memory segments that is available for data storage, wherein: each of the memory segments is associated with a respective second logic circuit having a first state when the memory segment of the block of memory segments is available for data storage and a second state when the memory segment of the block of memory segments is not available for data storage; and

the first state of the first logic circuit comprises a number of available memory segments in the block of memory segments, said number of available memory segments corresponding to the first state of each of the respective second logic circuits.

27. (Currently Amended) The method of claim 26, wherein the second state comprises ~~information indicating~~ an offset to available memory.

28-40. (Canceled)